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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,776	08/31/2001	Andrej Kocov	15311-2310	1813

7590 09/13/2005

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EXAMINER

PHAM, THOMAS K

ART UNIT PAPER NUMBER

2121

DATE MAILED: 09/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/944,776

Applicant(s)

KOCHEV ET AL.

Examiner

Thomas K. Pham

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 August 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 13-41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 13-36, 40 and 41 is/are rejected.
- 7) ☒ Claim(s) 37-39 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

Response to Amendment

1. This action is in response to the appeal brief filed on 08/11/2005.
2. In view of the Appeal Brief filed on 08/11/2005 , PROSECUTION IS HEREBY REOPENED. A new ground of rejection set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

- (1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,
- (2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Quotations of U.S. Code Title 35

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim Rejections - 35 USC § 103

5. Claims 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,119,185 (“Westerinen”) in view of U.S. Patent No. 6,718,413 (“Wilson”) and further in view of U.S. Patent no. 6,219,734 (“Wallach”).

Regarding claim 13

Westerinen teaches a method for programmably allocating system resources to accommodate I/O transactions at I/O ports (see abstract) of a multiprocessor computer system (see col. 1 line 61) comprising:

- setting criteria (configuring) for routing transactions (tasks) to the port with respect to the numbers of devices at the ports (see col. 2 lines 43-53 and col. 7 lines 21-33); and
- with respect to the numbers of devices at the ports, assigning devices to the ports (see col. 8 lines 25-37).

Westerinen does not teach determining the number of devices being serviced via the ports; identifying at least one assemblies for hot swapping; and copying the contents of cache memories associated with the at least one identified assemblies.

However, Wilson teaches determining the number of devices being serviced via the ports (col. 10 lines 34-42) for the purpose prioritizing the devices to reduce the number of interrupts (see col. 10 lines 29-30).

Furthermore, Wallach teaches identifying at least one assemblies for hot swapping (col. 17 lines 33-35); and copy the contents of old adapter to the new added adapter [port and adapter since they are both providing communication to I/O devices] (col. 12 lines 60-64) for the purpose of keeping track and allocates resources for every managed adapter (see col. 9 lines 18-20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the method of determining number of devices of Wilson with the method of Westerinen because it would provide for the purpose prioritizing the devices to reduce the number of interrupts.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the hot swapping method of Wallach with the method of Westerinen because it would provide for the purpose of keeping track and allocates resources for every managed adapter [port].

Regarding claim 15

Westerinen teaches a system for programmably allocating system resources to accommodate I/O transactions at I/O ports (see abstract) of a multiprocessor computer system (see col. 1 line 61), the system comprising:

- means for setting criteria (configuring) for routing transactions (tasks) to the port with respect to the numbers of devices at the ports (see col. 2 lines 43-53 and col. 7 lines 21-33); and
- means, responsive to the criteria, for assigning devices to the ports (see col. 8 lines 25-37).

Westerinen does not teach the means for determining the number of devices being serviced via the ports; at least one assemblies identified for hot swapping; and means for copying the contents of cache memories associated with the at least one identified assemblies.

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However, Wilson teaches determining the number of devices being serviced via the ports (col. 10 lines 34-42) for the purpose prioritizing the devices to reduce the number of interrupts (see col. 10 lines 29-30).

Furthermore, Wallach teaches at least one assemblies identified for hot swapping (col. 17 lines 33-35); and copy the contents of old adapter to the new added adapter [port and adapter since they are both providing communication to I/O devices] (col. 12 lines 60-64) for the purpose of keeping track and allocates resources for every managed adapter (see col. 9 lines 18-20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the system for determining number of devices of Wilson with the system of Westerinen because it would provide for the purpose prioritizing the devices to reduce the number of interrupts.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the hot swapping system of Wallach with the system of Westerinen because it would provide for the purpose of keeping track and allocates resources for every managed adapter [port].

Regarding claims 14 and 16

Wallach teaches assigning resources to the ports comprises at least one of assigning control registers to the ports, assigning direct memory access engines to the ports, assigning cache memory to the ports and assigning priorities among the transactions at the ports (col. 10 lines 58-61, "The configuration manager 500 ... adapter's configuration space registers").

Regarding claims 17 and 19

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Westerinen teaches a system determining the number and types of transactions anticipated at the ports, wherein the assignment of resources is further with respect to the numbers and types of transactions at the ports (col. 5 lines 38-46, "The Configuration Ruleset is ... provides a "parallel" implementation").

Regarding claims 18 and 20

Wallach teaches the at least one identified assembly has a memory system, and the method further comprises copying the states and status of the memory systems associated with at least one identified assembly (col. 9 lines 22-25, "The registers of an adapter 310 ... the status of the adapter").

6. Claims 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,119,185 ("Westerinen") in view of U.S. Patent No. 6,718,413 ("Wilson").

Regarding claim 21

Westerinen teaches a method for programmably allocating resources for processing Input/Output (I/O) transactions at a plurality of I/O ports of an I/O bridge (see abstract), the method comprising:

- setting criteria (configuring) for the transactions (tasks) at the at least one port with respect to the numbers of I/O devices being service at the ports (see col. 2 lines 43-53 and col. 7 lines 21-33); and
- assigning the resources to the at least one I/O port in response to the criteria (see col. 8 lines 25-37).

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Westerinen does not teach identifying the number of I/O devices being serviced by at least one I/O ports.

However, Wilson teaches identifying the number of I/O devices being serviced by at least one I/O ports (col. 10 lines 34-42) for the purpose prioritizing the devices to reduce the number of interrupts (see col. 10 lines 29-30).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the method of determining number of devices of Wilson with the method of Westerinen because it would provide for the purpose prioritizing the devices to reduce the number of interrupts.

Regarding claim 22

Westerinen teaches assigning a plurality of direct memory access (DMA) engines for use in processing I/O transactions (see col. 11 lines 7-11).

Regarding claim 23

Westerinen teaches apportioning a selected number of DMA engines to process a given transaction at a particular I/O port (see col. 5 lines 38-42).

Regarding claim 24

Westerinen teaches apportioning at least one DMA engine to process at least one transaction at a port (see col. 7 lines 21-33).

Regarding claim 25

Westerinen teaches apportioning one DMA engine to process a given transaction at a port identified as servicing multiple I/O devices (see col. 5 lines 38-42).

7. Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Westerinen in view of Wilson and further in view of U.S. Patent no. 6,085,294 ("VanDoren-94").

Regarding claim 26

Westerinen and Wilson teach a system for allocating resources but do not teach assigning at least one miss address file (MAF) value for processing I/O transactions. However, VanDoren-94 teaches at least one miss address file (MAF) (fig. 2 element 86a). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the MAF of VanDoren-94 with the system of Westerinen and Wilson because it would provide for processing I/O transactions data which has not yet completed by the CPU.

Regarding claim 27

VanDoren-94 teaches assigning a plurality of miss address file (MAF) values for processing I/O transactions (col. 7 lines 38-39, "Each CPU 12a-12d ... (MAF) 86a-86d").

Regarding claim 28

Westerinen, Wilson and VanDoren-94 teach a system for allocating resources with at least one MAF but do not teach reducing the assigned number of MAF. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to reduce or increase the number of MAF in accordance with the number of CPUs used.

8. Claims 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Westerinen in view of Wilson and further in view of U.S. Patent no. 6,085,276 ("VanDoren-76").

Regarding claim 29

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Westerinen and Wilson teach a system for allocating resources with the I/O bridge but do not teach configuring to utilize a plurality of virtual channels to communicate with at least one processors of a multiprocessor computer system, and the resources include flow control credits associated with each of the plurality of virtual channels. However, VanDoren-76 teaches a plurality of virtual channels to communicate with the multiprocessor system, and the resources include flow control credits associated with each of the plurality of virtual channels (col. 14 line 66 to col. 15 line 5, “ Virtual channels are a scheme ... among messages in the system”). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the virtual channels of VanDoren-76 with the system of Westerinen and Wilson because it would provide for eliminating flow-dependence and resource dependence cycles among messages in the system in order to eliminating deadlock in the cache coherence protocol.

Regarding claim 30

VanDoren-76 teaches setting the number of flow control credits associated with each virtual channel (col. 20 lines 14-20, “flow control from the ... in the SMP system”).

9. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,119,185 (“Westerinen”) in view of U.S. Patent No. 6,718,413 (“Wilson”) and further in view of U.S. Patent No. 6,219,734 (“Wallach”).

Regarding claim 31

Westerinen and Wilson do not teach the I/O bridge comprises at least one control register, the at least one control register having a plurality of fields, and at least one field of the

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control register being associated with a corresponding resource, and the method further comprises writing to a selected field of the at least one control register so as to modify the assignment of resources.

However, Wallach teaches the I/O bridge comprises at least one control register, the at least one control register having a plurality of fields, and at least one field of the control register being associated with a corresponding resource, and the method further comprises writing to a selected field of the at least one control register so as to modify the assignment of resources (col. 10 lines 57-61, "Once an adapter 310 ... configuration space registers") for the purpose of keeping track and allocates resources for every managed adapter (see col. 9 lines 18-20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the hot swapping method of Wallach with the method of Westerinen and Wilson because it would provide for the purpose of keeping track and allocates resources for every managed adapter [port].

10. Claims 32, 33, 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,219,734 ("Wallach") in view of U.S. Patent No. 6,119,185 ("Westerinen").

Regarding claim 32

Wallach teaches an Input/Output (I/O) bridge for use in a computer system having a plurality of processors, the I/O bridge comprising: a plurality of I/O ports, each I/O port configured to communicate with at least one I/O device that generates or receives transactions (col. 5 lines 1-5, "a programmable mass storage adapter ... the operational computer"); resources for use in

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servicing the transactions of the I/O devices (col. 10 lines 57-61, "Once an adapter 310 ... configuration space registers").

Wallace does not teaches a programmable logic configured and arranged to assign the resources among the I/O ports in response to the number of I/O devices with which the I/O ports are communicating.

However, Westerinen teaches a configuration logic that assign the resources among the I/O ports in response to the number of I/O devices (see col. 1 line 66 to col. 2 lines 12, "One embodiment of the Devices to that resource") for the purpose of efficiently and intelligently configures to achieve enhance performance and minimize conflicts (see col. 1 lines 49-52).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the configuration logic of Westerinen with the system of Wallach because it would provide for the purpose of efficiently and intelligently configures to achieve enhance performance and minimize conflicts.

Regarding claim 33

Westerinen teaches the resources comprise at least one direct memory access (DMA) engine configured to process the transactions (see col. 11 lines 7-11), and the programmable logic apportions the at least one of DMA engine to process at least one transaction at a given I/O port in response to the number of I/O devices coupled to the given I/O port (see col. 7 lines 21-33).

Regarding claim 40

Wallach teaches the configuration manager 500 comprises at least one control register associated with each I/O port, and the at least one control register has a first field for apportioning (col. 10 lines 58-61, "The configuration manager 500 ... adapter's configuration space registers").

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Westerinen teaches at least one apportioning at least one DMA engine to process at least one transaction at a port (see col. 7 lines 21-33).

Regarding claim 41

Wallace teaches the configuration manager 500 re-assigns resources among the I/O ports dynamically while the I/O bridge continues to operate (col. 10 lines 57-61, "Once an adapter 310 ... configuration space registers").

11. Claims 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallach in view of Westerinen and further in view of U.S. Patent no. 6,085,276 ("VanDoren-76").

Regarding claim 34

Wallach and Westerinen teach a system for allocating resources but do not teach the resources include a plurality of miss address file (MAF) values for use in requesting information from the computer system, and the programmable logic sets the number of available MAF values. However, VanDoren-94 teaches assigning a plurality of miss address file (MAF) values for processing I/O transactions (col. 7 lines 38-39, "Each CPU 12a-12d ... (MAF) 86a-86d"). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the MAF of VanDoren-94 with the system of Wallach and Westerinen because it would provide for processing I/O transactions data which has not yet completed by the CPU. Furthermore, it is obvious to one of ordinary skill in the art at the time the invention was made to reduce or increase the number of MAF in accordance with the number of CPUs used.

Regarding claim 35

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Wallach and Westerinen teach a system for allocating resources with the I/O bridge and a configuration manager 500 but do not teach the I/O bridge communicates with the computer system through a plurality of virtual channels, the resources include a plurality of flow control credits associated with the virtual channels, and the programmable logic assigns a number of flow control credits to each virtual channel. However, VanDoren-76 teaches a plurality of virtual channels to communicate with the multiprocessor system, and the resources include flow control credits associated with each of the plurality of virtual channels (col. 14 line 66 to col. 15 line 5, “Virtual channels are a scheme ... among messages in the system”) and setting the number of flow control credits associated with each virtual channel (col. 20 lines 14-20, “flow control from the ... in the SMP system”). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the virtual channels of VanDoren-76 with the system of Wallach and Westerinen because it would provide for eliminating flow-dependence and resource dependence cycles among messages in the system in order to eliminating deadlock in the cache coherence protocol.

Regarding claim 36

VanDoren-76 teaches the virtual channels comprise a Request channel, a Read I/O channel, and a Write I/O channel (col. 15 lines 16-28, “a Q0 channel for carrying ... from a processor to an IOP”).

Allowable Subject Matter

12. Claims 37-39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

In the remarks, applicants argue that prior art fail to teach:

- I. “setting criteria for transactions at a port, with respect to the number of devices being service via the ports” as to claim 13.
- II. “with respect to the number of devices, assigning resources to the ports” as to claim 13.
- II. “programmable logic configured and arranged to assign resources among I/O ports in response to the number of I/O devices with which the I/O ports are communicating” as to claim 32.

In response to applicants’ remarks:

- I. Prior art Westerinen (USPN 6,119,185 teaches configuring (setting criteria) the system with respect to the devices connected via the ISA, EISA and PCI adapters (ports) for executing the tasks (transactions) at the adapters (see col. 2 lines 43-53). The configuration rules (see col. 6, Table I) are applied for use in setting of these criteria appropriately with respect to the devices connected or being serviced at the adapters (ports).
- II. Furthermore, Westerinen teaches assigning the resources to the adapters based on the number of devices currently available for sharing (see col. 8 lines 25-37). The system is checking conflicts among the devices while allocates the resources to the devices at the ports.
- III. In addition, Westerinen teaches a logic that assign resources to the devices while the devices are being serviced at the ports (see col. 1 line 66 to col. 2 line 12). It is clear that the resources are assigning to the ports via the devices. Since the claim does not restrict on how the assignment of resources should be among the I/O ports nor required that the resources must be

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directly assigned to the port, assigning the resources to the port by way of the devices connected to the ports is the broadest reasonable interpretation of the claim.

Therefore, the limitations are taught by the reference presented in this Office Action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner *Thomas Pham*; whose telephone number is (571) 272-3689, Monday - Thursday from 6:30 AM - 5:00 PM EST or contact Supervisor *Mr. Anthony Knight* at (571) 272-3687.

Any response to this office action should be mailed to: **Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450**. Responses may also be faxed to the **official fax number (571) 273-8300**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas Pham
Patent Examiner



September 9, 2005



Anthony Knight
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